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Application No. 09853234 Prepared by	Tracking Number 0600, 8.106
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a. Serial No.	f. Foreign Priority	k. Print Claim(s)	PTO-1449			
b. Applicant(s)	g. Disclaimer	I. Print Fig.	q. PTOL-85b			
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract			
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs			
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other			

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ist of Patents and Publications for Applicant's

Atty. Docket No. 2000.080000/TT4828

Serial No. 09/853,234

Applicant Strongin et al.

Information Disclosure Statement

(Use several sheets if necessary)

Filing Date: May 11, 2001 Group: 2185

U.S. Patent Documents

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Foreign Patent Documents
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Other Art See Page 1

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
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	A2					REC	EVED
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-	B2						
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	Cl	Intel, "Low Pin Count (LPC) Interface Specification Revision 1.0," pp. 1-31 (09/29/97)			
	C2	Standard Microsystems Corporation, "100 Pin Enhanced Super I/O for LPC Bus with SMBus Controller for Commercial Application," Part No. LPC47B37x, pp. 1-254 (06/17/99)			
- <u></u>	C3	FIPS Pub 140-1 Federal Information Processing Standards Publication, "Security Requirements for Cryptographic Modules" (01/11/1994)			
	C4	Intel, "Communication and Networking Riser Specification," Revision 1.0 (02/07/2000)			
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